WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a plurality of first regions arranged along a first direction, each of which corresponds to a memory array including a plurality of word lines extending in a second direction perpendicular to said first direction, a plurality of bit lines extending in said first direction and a plurality of memory cells; and

a plurality of second regions, each of which is arranged alternately with respect to each of said first regions arranged along said first direction and each including sense amplifiers connected to said bit lines to form an open bit line type semiconductor memory,

wherein two of the first regions at end portions of said plurality of first regions are both selected together, and

wherein one of the first regions at an inner portion of said plurality of first regions is selected independently.

2. A semiconductor memory according to claim 1,

wherein one of said word lines in a selected first region is activated.

3. A semiconductor memory comprising:

a plurality of memory arrays arranged along a first direction, each of which includes a plurality of word lines extending in a second direction perpendicular to said first direction, a plurality of bit lines extending in said first direction and a plurality of dynamic memory cells; and

a plurality of sense amplifiers, each of which is arranged alternately with respect to each of said memory arrays arranged along said first direction, each of which sense amplifier includes latch circuits connected to said bit lines to form an open bit line type semiconductor memory,

wherein two memory arrays at end portions of the plurality of memory arrays are both selected together,

wherein one of the memory arrays at an inner portion of the plurality of memory arrays is selected independently, and

wherein one of said word lines in a selected memory array is activated.